WHAT IS CLAIMED IS:

1. A cryptographic system comprising:

a first FIFO data storage device having a primary write address to receive unprocessed data via a first data path into the first FIFO data storage device, a primary read address, a secondary read address and a secondary write address; and

an encryption/decryption circuit configured to read the unprocessed data via the secondary read address, selectively encrypt or decrypt the unprocessed data read via the secondary read address to generate processed data, and write the processed data back into the first FIFO data storage device via the secondary write address, such that the processed data written back into the first FIFO data storage device can be read from the first FIFO data storage device via the primary read address.

2. The cryptographic system according to claim 1 wherein the FIFO data storage device is a single port random access memory.

3. The cryptographic system according to claim 1 further comprising:

a second FIFO data storage device having a primary write address to receive unprocessed data via a second data path into the second FIFO data storage device, a primary read address, a secondary read address and a secondary write address; and

a switching circuit configured to multiplex between the first and second FIFO data storage devices such that the encryption/decryption circuit can parallel process the unprocessed data stored in the first and second FIFO data storage devices to generate respective processed data, and write the respective processed data back into the first and second FIFO data storage devices via their respective secondary write addresses, such that the respective processed data written back into the first and second FIFO data storage devices can be read from the first and second FIFO data storage devices via their respective primary read addresses.

4. The cryptographic system according to claim 3 wherein the first and second FIFO data storage devices each comprise a single port random access memory.

5. A cryptographic system comprising:

a first single port random access memory (RAM) configured with a primary write address to receive unprocessed data via a first data path into the single port RAM, a primary read address, a secondary read address and a secondary write address; and

an encryption/decryption circuit configured to read the unprocessed data via the secondary read address, selectively encrypt or decrypt the unprocessed data read via the secondary read address to generate processed data, and write the processed data back into the first single port RAM via the secondary write address, such that the processed data written back into the first single port RAM can be read from the first single port RAM via the primary read address.

6. The cryptographic system according to claim 5 further comprising:

a second single port RAM having a primary write address to receive unprocessed data via a second data path into the second single port RAM, a primary read address, a secondary read address and a secondary write address; and

a switching circuit configured to multiplex between the first and second single port RAMs such that the encryption/decryption circuit can parallel process the unprocessed data stored in the first and second single port RAMs to generate respective processed data, and write the respective processed data back into the first and second single port RAMs via their respective secondary write addresses, such that the respective processed data written back into the first and second single port RAMs can be read from the first and second single port RAMs via their respective primary read addresses.

7. A cryptographic system comprising a first FIFO memory configured with a primary write address to receive unprocessed data into the first FIFO memory via a first data path, a secondary read address to provide access to the unprocessed data such that an external user can retrieve and encrypt or decrypt the unprocessed data, a secondary write address to receive data back into the first FIFO memory that has first been read from the first FIFO memory and encrypted or decrypted, and a primary read address to provide access to data that has been read from the first FIFO memory, encrypted or decrypted, and written back into the first FIFO memory via the secondary write address.

8. The cryptographic system according to claim 7 wherein the first FIFO memory is a single port random access memory.

9. The cryptographic system according to claim 7 further comprising an encryption/decryption circuit configured to read the unprocessed data stored in the first FIFO memory via the secondary read address, selectively encrypt or decrypt the unprocessed data that has been read to generate processed data, and write the processed data back into the first FIFO memory via the secondary write address, such that the processed data written back into the first FIFO memory can be read from the first FIFO memory via the primary read address.

10. The cryptographic system according to claim 9 wherein the first FIFO memory is a single port random access memory.

11. The cryptographic system according to claim 9 further comprising:

a second FIFO memory having a primary write address to receive unprocessed data via a second data path into the second FIFO memory, a primary read address, a secondary read address and a secondary write address; and

a switching circuit configured to multiplex between the first and second FIFO memory such that the encryption/decryption circuit can parallel process the unprocessed data stored in the first and second FIFO memory to generate respective processed data, and write the respective processed data back into the first and second FIFO memory via their respective secondary write addresses, such that the respective processed data stored in the first and second FIFO memory can be read from the first and second FIFO memory via their respective primary read addresses.

12. The cryptographic system according to claim 11 wherein the first and second FIFO memory each comprise a single port random access memory.

13. A method of performing data cryptography comprising the steps of:

providing a first FIFO memory having a primary write address, a secondary read address, a primary read address, and a secondary write address;

writing data into the first FIFO memory via the primary write address;

reading the written data via the secondary read address;

selectively encrypting or decrypting the read data to generate processed data; and

writing the processed data into the first FIFO memory via the secondary write address.

14. The method according to claim 13 further comprising the step of reading the written processed data via the primary read address.

15. A method of performing data cryptography comprising the steps of:

providing a first FIFO memory having a primary write address, a secondary read address, a primary read address, and a secondary write address;

writing data into the first FIFO memory via its primary write address;

providing a second FIFO memory having a primary write address, a secondary read address, a primary read address, and a secondary write address;

writing data into the second FIFO memory via its primary write address;

providing a switcher configured to multiplex between the first and second FIFO memory secondary read addresses and the first and second FIFO memory secondary write addresses;

multiplexing between the first and second FIFO memory secondary read addresses to selectively access the data written into the first and second FIFO memories;

selectively encrypting or decrypting the multiplexed data to generate processed data;

writing processed data generated from data stored in the first FIFO memory back into the first FIFO memory via its secondary write address; and

writing processed data generated from data stored in the second FIFO memory back into the second FIFO memory via its secondary write address.

16. The method according to claim 15 further comprising the step of reading the processed data written back into the first FIFO memory via its primary read address.

17. The method according to claim 15 further comprising the step of reading the processed data written back into the second FIFO memory via its primary read address.